What is claimed is:

1. A semiconductor device test pattern, comprising:

a word line on a semiconductor substrate;

an active region comprising a first impurity doped region and a second impurity doped region;

a first self-aligned contact pad electrically connected to the first impurity doped region;

a first bit line electrically connected to the first self-aligned contact pad;

a first probing pad electrically connected to the first bit line;

a second self-aligned contact pad electrically connected to the second impurity doped region;

a second conductive line electrically connected to the second self-aligned contact pad; and

a second probing pad electrically connected to the second conductive line.

2. The semiconductor device test pattern of Claim 1, further comprising:

a first direct contact electrically connected to the first self-aligned contact pad; and

a second contact electrically connected to the second self-aligned contact pad;

3. The semiconductor device test pattern of Claim 1, wherein the first self-aligned contact pad is one of a plurality of discrete first self-aligned contact pads disposed between the word line and a second word line.

4. The semiconductor device test pattern of Claim 1, further comprising an insulating pattern disposed between each of the first self-aligned contact pads disposed between the word line and a second word line.

5. The semiconductor device test pattern of Claim 1, further comprising a first metal contact between the first bit line and the first probing pad that electrically connects the first bit line and the first probing pad.

6. The semiconductor device test pattern of Claim 1, further comprising a second metal contact between the second conductive line and the second probing pad that electrically connects the second conductive line and the second probing pad.

7. The semiconductor device test pattern of Claim 1, wherein the second impurity doped region is one of a plurality of second doped impurity regions disposed between the word line and a second word line, and wherein the second self-aligned contact pad extends in a continuous line between the word line and the second word line to electrically connect to the plurality of second impurity doped regions.

8. The semiconductor device test pattern of Claim 1, wherein the first bit line is perpendicular to a major axis of the active region.

9. The semiconductor device test pattern of Claim 1, wherein the second conductive line is a second bit line that is perpendicular to the word line.

10. The semiconductor device test pattern of Claim 2, wherein the second contact is a buried contact.

11. The semiconductor device test pattern of Claim 1, wherein a major axis of the active region is at an oblique angle with respect to the word line.

12. The semiconductor device test pattern of Claim 1, wherein the second conductive line is a second bit line that is parallel to the word line.

13. The semiconductor device test pattern of Claim 1, wherein the first bit line and the second conductive line have a plurality of arms, and wherein one of the arms of the first bit line is disposed between each adjacent set of arms of the second conductive line.

14. The semiconductor device test pattern of Claim 1, wherein the second self-aligned contact pad is one of a plurality of discrete second self-aligned contact pads disposed between the word line and a second word line.

15. The semiconductor device test pattern of Claim 13, wherein the second impurity doped region is one of a plurality of discrete second impurity doped regions disposed between the word line and the second word line, and wherein each of the second self aligned contact pads electrically connects to two of the discrete second impurity doped regions.

16. The semiconductor device test pattern of Claim 3, wherein the second

self-aligned contact pad is one of a plurality of discrete second self-aligned contact pads disposed between the word line and a second word line, and wherein the one of the plurality of second self-aligned contact pads is disposed between adjacent of the first self-aligned contact pads.

17. A method of forming a semiconductor device test pattern, the method comprising:

forming a word line on a semiconductor substrate;

forming a first impurity doped region and a second impurity doped region at the semiconductor substrate;

forming a first self-aligned contact pad electrically connected to the first impurity doped region and a second self-aligned contact pad electrically connected to the second impurity doped region;

forming a first direct contact electrically connected to the first self-aligned contact pad and a second contact electrically connected to the second self-aligned contact pad;

forming a first bit line electrically connected to the first direct contact;

forming a second conductive line electrically connected to the second contact;

forming a first metal contact electrically connected to the first bit line and a second metal contact electrically connected to the second conductive line; and

forming a first probing pad electrically connected to the first metal contact and a second probing pad electrically connected to the second metal contact.

18. The method of Claim 17, further comprising forming a first interlayer dielectric layer on the semiconductor substrate, forming a second interlayer dielectric layer on the first interlayer dielectric layer, and forming a third interlayer dielectric layer on the second interlayer dielectric layer, and wherein the first self-aligned contact pad penetrates the first interlayer dielectric layer to electrically connect to the first impurity doped region and the second self-aligned contact pad penetrates the first interlayer dielectric layer to electrically connect to the second impurity doped region, and wherein the first direct contact penetrates the second interlayer dielectric layer to electrically connect to the first self-aligned contact pad and the second contact penetrates the second interlayer dielectric layer to electrically connect to the second self-aligned contact pad.

19. The method of Claim 18, wherein the second direct contact further penetrates the third interlayer dielectric layer so that the second contact is a buried contact.

20. The method of Claim 18, wherein the first metal contact penetrates the third interlayer dielectric layer to electrically connect to the first bit line and the second metal contact penetrates the third interlayer dielectric layer to electrically connect to the second conductive line.

21. The method of Claim 18, further comprising a fourth interlayer dielectric layer on the third interlayer dielectric layer, and wherein the first metal contact penetrates the fourth and third interlayer dielectric layers to electrically connect to the first bit line and the second metal contact penetrates the fourth interlayer dielectric layer to electrically connect to the second conductive line.

22. The method of Claim 17, wherein the second conductive line is a bit line.

23. The method of Claim 17, wherein the second conductive line is a probing line.

24. The method of Claim 17, wherein the first impurity doped region and the second impurity doped region form an active region having a major axis, and wherein the major axis of the active region is at an oblique angle with respect to the word line.

25. The method of Claim 24, wherein the first bit line and the second conductive line each extend at a right angle to the major axis of the active region.

26. The method of Claim 17, wherein the first self-aligned contact pad is one of a plurality of discrete first self-aligned contact pads disposed between the word line and a second word line.

27. The method of Claim 17, wherein the second impurity doped region is one of a plurality of second doped impurity regions disposed between the word line and a second word line, and wherein the second self-aligned contact pad extends in a continuous line between the word line and the second word line to electrically connect

to the plurality of second doped impurity regions.

28. The method of Claim 17, wherein the second conductive line is parallel to the first bit line.

29. The method of Claim 17, wherein the second conductive line is perpendicular to the first bit line.

30. The method of Claim 17, wherein the first bit line and the second conductive line have a plurality of arms, and wherein one of the arms of the first bit line is disposed between each adjacent set of arms of the second conductive line.

31. The method of Claim 17, wherein the second self-aligned contact pad is one of a plurality of discrete second self-aligned contact pads disposed between the word line and a second word line.

32. The method of Claim 31, wherein the second impurity doped region is one of a plurality of discrete second impurity doped regions disposed between the word line and the second word line, and wherein each of the second self aligned contact pads electrically connects to two of the discrete second impurity doped regions.

33. The method of Claim 26, wherein the second self-aligned contact pad is one of a plurality of discrete second self-aligned contact pads disposed between the word line and a second word line, and wherein the one of the plurality of second self-aligned contact pads is disposed between adjacent of the first self-aligned contact pads.

34. A method of measuring leakage current between a first impurity doped region and a second impurity doped region of a cell transistor in a semiconductor device, the method comprising:

electrically connecting a first probing pad to the first impurity doped region via a first contact pad and a first bit line;

electrically connecting a second probing pad to the second impurity doped region via a second contact pad and a second conductive line; and

measuring the leakage current of the cell transistor by measuring the current flowing between the first probing pad and the second probing pad.

35. The method of Claim 34, wherein a first direct contact is further included in the electrical path between the first probing pad and the first impurity doped region.

36. The method of Claim 35, wherein a second contact is further included in the electrical path between the second probing pad and the second impurity doped region.

37. The method of Claim 34, wherein the second conductive line comprises a second bit line and wherein the second contact pad electrically connects to a plurality of impurity doped regions associated with a plurality of other cell transistors of the semiconductor device.

38. The method of Claim 36, wherein the second contact comprises a buried contact and wherein the second conductive line comprises a probing line that electrically connects to a plurality of buried contacts associated with a plurality of other cell transistors of the semiconductor device.

39. The method of Claim 34, wherein the first bit line and the second conductive line each form an oblique angle with respect to an active region defined by the first impurity doped region and the second impurity doped region.

40. The method of Claim 39, wherein the second contact pad further electrically connects to an impurity region associated a second cell transistor of the semiconductor device.

41. A semiconductor test structure comprising:

a semiconductor substrate including a plurality of active regions separated by isolation regions;

a plurality of parallel word lines on the semiconductor substrate with each word line crossing a plurality of the active regions;

an array of transistors on the semiconductor substrate, wherein each transistor of the array includes first and second source/drain regions on opposite sides of a respective of the plurality of word lines, wherein each word line separates the first and second source/drain regions of a plurality of the transistors of the array, and wherein

each active region includes two transistors of the array sharing a common source/drain region;

a first bit line electrically connected to a first source/drain region of each transistor of the array; and

a second conductive line electrically connected to a second source/drain region of each transistor of the array.

42. A semiconductor test structure according to Claim 41 wherein the semiconductor substrate further includes a plurality of dynamic random access memory devices thereon.